**EAST WEST UNIVERSITY**

**Department of Computer Science & Engineering**

**Semester:** Fall 2017

**Course Number:** CSE 345

**Course Title:** Digital Logic Design

**Experiment No:** 01

**Experiment Title:** Schematic and Structural Verilog Simulation of

Combination Logic Circuits

**Name:** Md. Sakibur Rahman  
**ID:** 2014-1-60-032

**Group Number:** 01  
**Group IDs:**  
2014-1-60-032  
2015-1-60-065  
2015-1-60-071  
2015-1-60-081

**Date of Performance:** September 25, 2017

**Date of Report Submission:** October 2, 2017

**Post Lab - 1 Report**

**Objectives:**

1. To learn schematic simulation of combinational logic circuits using Quartus II software.
2. To learn structural Verilog simulation of combinational logic circuits using Quartus II software.

**Answers to the Post-Lab Questions:**

Simulation and truth table result comparison

|  |  |
| --- | --- |
| **Simulation** | **Truth Table** |
| 0 | 0 |
| 1 | 1 |
| 1 | 1 |
| 0 | 0 |
| 1 | 1 |
| 0 | 0 |
| 0 | 0 |
| 1 | 1 |

**Conclusion:**

For getting the output of a combinational circuit we used Boolean expression and truth table in this experiment. Using Quartus II software we wrote here structural Verilog code and then simulated the code successfully.